IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)	
	)	
Bains et al. for	)	
Intel Corporation	)	
	)	
Serial No.: 10/750,154	)	Group Art Unit: 2186
	)	
Filed: December 31, 2003	)	Examiner: IWASHKO, LEV

For: **Method And Apparatus To Counter Mismatched Burst Lengths**

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter Appellants) submit this appeal brief, thus perfecting the notice of appeal filed on November 27, 2006. The required headings and subject matter follow.

Filed EFS- WEB on January 26, 2007

(i) Real party in interest.

This case is assigned of record to Intel Corporation, who is the real party in interest.

(ii) Related appeals and interferences.

There are no known related appeals and/or interferences.

(iii) Status of claims.

Claims 1-20 are pending and stand rejected. Claims 1-20 are being appealed.

(iv) Status of Amendments.

An After Final Response that amended claim 1 was mailed November 27, 2006. The appendix reflects the entry of entered amendment to claim 1.

(v) Summary of claimed subject matter.

Paragraph numbering of the filed application and the published application may differ. Accordingly, the following description references paragraphs of the present application based upon the paragraph numbering of the application as published. The supplied reference numbers and paragraphs are not meant to limit the scope of the present claims but merely to provide examples of some elements to aid understanding. The actual claim scope may be broader and/or narrower than the example elements given.

Claim 1 relates to a memory IC 170 comprising a control logic 173 shared by both the first and second groups 185a-d and 195a-d, coupled to both the first and second row address decoders 182a-d and 192a-d, coupled to both the first and second bank selection logics 181 and 191, storing information concerning the state of all banks in the first group, including the first bank, and separately storing information concerning the state of all banks in the second group, including the second bank (See FIG. 1, paragraph [0014], lines 7-11 in page 11, para [0015], lines 14-17 in page 12, para [0021], lines 7-9 in page 16 and FIG. 2, para [0026], lines 10-12 in page 20). The memory IC further comprises a data buffer 178 shared by both the first and second groups 185a-d and 195a-d of banks of memory (See FIG. 1, paragraph [0014], lines 7-11 in page 11).

Claim 4 relates to the memory IC of claim 1, wherein the control logic 273 stores information concerning which rows are open in all banks in the first group 286 separately from information concerning which rows are open in all banks in the second group 296 (See FIG. 2, paragraph [0021], lines 7-14 in page 16).

Claim 6 relates to an electronic system comprising a control logic shared by both the first and second group of memory banks and having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group (See FIG. 1, paragraph [0014], lines 7-11 in page 11, para [0015], lines 14-17 in page 12, para [0021], lines 7-9 in page 16 and FIG. 2, para [0026], lines 10-12 in page 20). The electronic system further comprises a memory controller 251 having

a third state logic storing information concerning the state of all banks in the first group within the memory IC, and having a fourth state logic storing information concerning the state of all banks in the second group within the memory IC (See FIG.2, para [0023, lines 7-16 in page 17).

Claim 10 relates to the electronic system of claim 6, wherein the memory controller 551 incorporates a control storage to maintain information concerning the size of a cache line within the cache. (See FIG. 5, paragraphs [0035], lines 28-29 in page 24).

Claim 11 relates to the electronic system of claim 6, wherein the control logic 273 stores information concerning which rows are open in all banks in the first group 286 separately from information concerning which rows are open in all banks in the second group 296 (See para [0015], lines 3-14 in page 12, para [0021], lines 7-10 in page 16 and para [0024], lines 3-14 in page 18).

Claim 13 relates to the electronic system of claim 6, wherein the memory controller signals the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction (See para [0017], lines 3-9 and lines 21-29 in page 13). Further, the memory controller, of the electronic system, times the first and second read transactions to minimize the time that elapses between the end of the actual transfer of bytes across the memory bus for the first read transaction and the beginning of the actual transfer of bytes across the memory bus for the second read transaction (See para [0017], lines 4-8 in page 14).

Claim 16 relates to a method comprising waiting a period of time appropriate to prevent conflicts between transfers of bytes for the first and second read operations and to minimize the amount of time between the ends of the burst transfer of data for the first read operation to the beginning of the burst transfer of

data for the second read operation (See FIG. 2, para [0024], lines 7-9 in page 18 and FIG. 6, para [0036], lines 12-15 in page 25). The method further comprises transmitting first read command of the first read operation to the memory IC and second read command for the second read operation to the memory IC (See FIG. 6 para 36, lines 9-11 and line 16-21 in page 25).

Claim 17 relates to a method of claim 16, further comprising checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations (See para [0026], lines 25-29 in page 19 and lines 1-10 in page 20).

Claim 20 relates to a machine accessible medium comprising code that when executed by a processor within an electronic system, causes the electronic system to check the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in a memory device that possesses such independently operable groups of banks of memory cells (See para [0026], lines 25-29 in page 19 and lines 1-10 in page 20). The machine accessible medium code further comprises to determine a quantity of bytes to which to limit the burst transfer of bytes of data in a read transaction from a memory device that possesses such independently operable groups of banks of memory cells (See para [0017], lines 3-9 and lines 21-29 in page 13).

(vi) Grounds of rejection to be reviewed on appeal

Whether claims 1-3, 5-8 and 12 are anticipated under 35 U.S.C. §102(b) by Jung-bae Lee et al. (US Patent No. 6,151,271).

Whether claims 4 and 11 are unpatentable under 35 U.S.C. §103(a) over Jung-bae Lee in view of Ho-cheol Lee (US Patent No. 6,279,116).

Whether claim 10 is unpatentable under 35 U.S.C. §103(a) over Jung-bae Lee, in view of Carnevale et al. (US Patent No. 5,721, 874).

Whether claims 13, 14 and 15 are unpatentable under 35 U.S.C. §103(a) over Jung-bae Lee, in view of Kopet at al. (US Patent No. 4,448,310).

Whether claim 16 is unpatentable under 35 U.S.C. §103(a) over Jung-bae Lee, in view of "Bit Vector Algorithm for Detecting Self-Data Chains" (hereafter referred to as "IBM").

Whether claims 18 and 19 are unpatentable under 35 U.S.C. §103(a) over Jung-bae Lee and IBM, in view of Kopet at al. (US Patent No. 4,448,310).

Whether claim 20 is unpatentable under 35 U.S.C. §103(a) over Kopet et al. in view of Ho Cheol Lee, Keskar et al. Carnevale et al. and IBM.

(vii) Argument.

Claim Rejections under 35 USC § 102 (Jung-bae Lee)

The rejection of claims 1-3, 5-8 and 12, under 35 U.S.C. §102(b), as being anticipated by Jung-bae Lee (US Patent No. 6,151,271), is in error and should be reversed.

As is well-established, in order to successfully assert a *prima facie* case of anticipation, the Official Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Official Action has not succeeded in making a prima facie case.

Claim 1

Claim 1 requires a control logic shared by both the first and second groups of banks of memory and coupled to both the first and second row address decoders. The control logic also coupled to both the first and second bank selection logics and

stores information concerning the state of all banks in the first and second group separately.

In column 1, lines 66-67 to column 2, lines 1-29, Jung-bae Lee discloses an integrated circuit memory device which include first and second memory banks, first and second local data lines electrically coupled to the first and second memory bank, respectively, and a multiplexer having first and second inputs electrically coupled to first and second data bus line. A data selection circuit is also provided to route data from the first and second local data lines to the first and second data bus lines, respectively, when a selection control signal is in a first logic state. The data selection circuit routes data from the second and first local data lines to the first and second data bus lines, respectively, when a selection control signal is in a second logic state opposite to the first logic state. A control signal generator also provided to generate selection control signal in the first and second logic states when a first address in a string of burst addresses is even and odd, respectively.

In column 4, lines 3-17, Jung-bae Lee discloses that the data selection circuit 45 includes first and second I/O sense amplifiers 40 and 42 and first and second data bus selectors 44 and 46. The I/O sense amplifiers receive even and odd data from the memory core and loaded on the local input output lines, amplify the data and outputs the amplified data on global input and output lines in response to the control signals. Similarly, the data bus selectors receive even and odd data from I/O amplifiers and select even or odd data in response to the complementary selection control signal (See column 4, lines 36-52). Thus, the data selection circuit is to

receive even and odd data, amplify even and odd data and select amplified data in response to selection control signals, but dos not appear to store data and be shared by the groups of banks of memory.

The Final Office Action appears to rely upon the **data selection circuit/control signal generator** of Jung-bae Lee for a teaching of the **control logic** of the Appellant's invention of claim 1. Appellants submit that the data selection circuit routs even and odd data in first and second logic state in response to selection control signals generated by the control signal generator in the first and second logic state, amplify even and odd data and select amplified data. The data selection circuit/control signal generator does not appear to be coupled to both the first and second row address decoders and first and second bank selection logics. Also, the data selection circuit/control signal generator does not appear to store information concerning the state of all banks in the first and second group, separately. In contrast, the control logic of Appellant's invention may be shared by both the groups of banks of memory and may store information concerning the state of all banks in the first group and second group, separately. Further, the control logic may be coupled to both the first and second bank selection logics and first and second row address decoders.

In the advisory action, the Examiner has asserted that a person skilled in the art would have considered the data selection circuit of Jung-bae Lee with Appellant's claimed control logic depending on the functions. Appellants submit that even if it is presumed that the data selection circuit of Lee is similar to the control logic disclosed

by the Appellant's claim 1, Lee still does not teach that the data selection circuit can be shared by both the groups of banks of memory, may be coupled to both first and second bank selection logics and may store information concerning the state of all banks in the first group and second group, separately.

Appellants submit that the data selection circuit/control signal generator of Lee does not appear to perform the functions as performed by the control logic of present invention and hence data selection circuit is not the same even functionally to the control logic of the Appellants. Appellants do not believe that the data selection circuit of Lee, which is meant to route even and odd data in the first and second logic state in response to selection control signals, anticipates the control logic of the Appellants, which may be shared by both the groups of banks of memory, may be coupled to both first and second bank selection logics and may store information concerning the state of all banks in the first group and second group, separately.

Further, in column 3, lines 9-44 and as shown in FIG. 1, Lee discloses a synchronous DRAM which includes a plurality of memory cell arrays and each memory cell array include a plurality of memory cell sub-arrays. The office action appears to equate DRAM of Lee with control logic of the Appellant's claim 1. Unlike the DRAM, the control logic of the Appellant's invention may be shared by both the first and second groups of banks of memory. Further, Appellants submit that a person skilled in the art would not consider DRAM of Lee similar to the control logic of the Appellant's claim 1.

Since, Jung-bae Lee does not teach each and every element of Appellant's claim 1, Lee does not anticipate Appellant's invention of claim 1. Appellants respectfully request the rejection of claim 1 be reversed.

Claims 2, 3 and 5

Each of the claims 2, 3 and 5 depends from claim 1. Accordingly, each of the claims 2, 3 and 5 is allowable for at least the reasons stated above in regard to claim 1. Appellants submit that the above submissions are sufficient to overcome the present rejection of claims 2, 3 and 5 under Lee. Appellants respectfully request that the rejection of claims 2, 3 and 5 be reversed.

Claim 6

Claim 6 requires a control logic shared by both the first and second group of memory banks and having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group.

As discussed above in column 1, lines 66-67 to column 2, lines 1-16, Lee discloses an integrated circuit memory device which includes first and second memory banks. First and second local data lines are electrically coupled to the first and second memory bank. A multiplexer having first and second inputs are electrically coupled to first and second data bus line. A data selection circuit is provided to route data from the first and second local data lines to the first and second data bus lines, respectively, when a selection control signal is in a first logic

state. The data selection circuit also routes data from the first and second local data lines to the first and second data bus lines, when a selection control signal is in a second logic state opposite the first logic state. Also, in column 3, lines 9-44 and as shown in FIG. 1, Lee discloses a synchronous DRAM which includes a plurality of memory cell arrays and each memory cell arrays include a plurality of memory cell sub- arrays.

Appellants have been unable to locate where Lee teaches a control logic having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group. Appellants submit that Lee appears to teach features and functioning of the integrated circuit memory devices and synchronous DRAM, but does not teach anything regarding the control logic as required by the Appellant's claim 6. Further, Appellants submit that the above arguments with regard to claim 1 are applicable to the patentability of claim 6.

Since, Lee does not teach each and every element of Appellant's claim 6, Lee does not anticipate Appellant's claim 6. Appellants respectfully request that the rejection of claim 6 be reversed.

Claims 7, 8 and 12

Each of the claims 7, 8 and 12 depends from claim 6. Accordingly, each of the claims 7, 8 and 12 is allowable for at least the reasons stated above in regard to claim 6. Appellants respectfully submit that the above submissions are sufficient to

overcome the present rejection of claims 7, 8 and 12 under Lee. Appellants respectfully request that the rejection of claims 7, 8 and 12 be reversed.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/Ho-Cheol Lee)

The rejection of claims 4, 9 and 11 under 35 U.S.C. § 103(a), as being unpatentable over Jung-bae Lee as applied to claim 1 and 6 above, further in view of Ho-Cheol Lee (US Patent 6,279,116B1), is in error and should be reversed.

Claims 4 and 11

Claims 4 and 11 include claim 1 and claim 6 as a base claim, respectively. Accordingly, claims 4 and 11 are allowable for at least the reasons stated above in regard to claims 1 and 6. Furthermore, claims 4 and 11 require control logic to store information concerning which rows are open in all banks in the first group separately from information concerning which rows are open in all banks in the second group.

In column 13, line 45-49, Ho-Cheol Lee discloses that the row control circuit is meant for generating signals or clocks for selecting word line during time period of t_{RCD} and developing to bit lines information data from memory cells in a read operation. Also, the row control circuit is meant for precharging during the time period of t_{RP}. However, Appellants have been unable to locate where Ho-Cheol Lee teaches the control logic to store information concerning which rows are open in all banks in the first group separately from information concerning which rows are open in all banks in the second group.

The Final Office Action appears to rely upon the **row control circuit** of Ho-Cheol Lee for a teaching of the **control logic** to store information as required by the Appellant's invention of claims 4 and 11. Ho-Cheol Lee teaches that row control circuit is meant for generating signals or clocks for selecting word line during time period of t_{RCD}, developing to bit lines information data from memory cells in a read operation and for precharging during the time period of t_{RP}. In contrast, the control logic of the Appellant's invention is to store the information relating to rows open in all banks in the first and second group separately and the read/write operation is directed to the intended row by the control logic. Jung-bae Lee also does not teach the invention of claims 4 and 11.

Appellants respectfully submit that the proposed combination of Jung-bae Lee and Ho-Cheol Lee does not teach each and every element of Appellant's claims 4 and 11, the proposed combination does not arrive at the invention of the Appellant's claims 4 and 11. Appellants respectfully request that the rejection of claims 4 and 11 be reversed.

Claim 9

Claim 9 include claim 6 as a base claim. Accordingly, claim 9 is allowable for at least the reasons stated above in regard to claim 6. Appellants submit that the above submissions are sufficient to overcome the present rejection of claim 9 under Jung-bae Lee and Ho-Cheol Lee.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/Carnevale)

The rejection of claim 10 under 35 U. S. C. 103 (a), as being unpatentable over Jung-bae Lee as applied to claim 6 and 9 above, further in view of Carnevale et al. (US Patent 5,721,874), is in error and should be reversed.

Claim 10 include claim 6 as a base claim. Accordingly, claim 10 is allowable for at least the reasons stated above in regard to claim 6. Appellants submit that the above arguments are sufficient to overcome the present rejection of claim 10 under Jung-bae Lee and Carnevale. Appellants respectfully request that the rejection of claim 10 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/Kopet)

The rejection of claims 13-15 under 35 U. S. C. 103 (a), as being unpatentable over Jung-bae Lee as applied to claim 6 and 12 above, further in view of Kopet et al. (US Patent 5,448,310), is in error and should be reversed.

Claim 13

Claim 13 includes claim 6 as a base claim. Accordingly, claim 13 is allowable for at least the reasons stated above in regard to claim 6. Furthermore, claim 13 requires the memory controller to signal the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction.

Kopet discloses the difference between mode 1 and mode 0 burst read cycles (FIG. 31) and termination of the Mode 1 and Mode 0 burst read cycles, based on the assertion and deassertion of the number of words set for the termination of Mode burst read cycles. However, Kopet does not teach that a memory controller signals the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction. Additionally, Kopet does not appear to teach that the memory controller times the first and second read transactions to minimize the time that elapses between the end of the actual transfer of bytes across the memory bus for the first read transaction and the beginning of the actual transfer of bytes across the memory bus for the second read transaction as required by the Appellant's claim 13.

As conceded in the office action, Jung-bae Lee also does not teach that the memory controller signals the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction.

As is well established, a prima facie showing of obviousness may only be established if there is a clear suggestion from or in the prior art to make the modifications proposed by the Examiner. *See Gillette Co. v. S.C. Johnson & Son, Inc.* 919 F. 2d 720 (Fed Cir. 1990). Appellants submit that there is no clear suggestion or motivation, in the light of the cited references, for a person to combine the references. The Final Official Action appears to combine the "Integrated Memory

Circuit Device" of Jung-bae Lee and "Motion Estimation Coprocessor" of Kopet in order to propose an early termination of first and second read transactions. Despite the broad statement made by the Examiner, there appears to be no motivation for one skilled in the art to make the proposed combination.

Since, the proposed combination does not teach the memory controller to signal the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction, the proposed combination does not arrive at the invention of the Appellant's claim 13. Appellants respectfully request that the rejection of claim 13 be reversed.

Claims 14-15

Claims 14-15 include claim 13 as a base claim. Accordingly, claims 14-15 are allowable for at least the reasons stated above in regard to claim 13. Appellants submit that the above arguments are sufficient to overcome the present rejection of claims 14-15 under Jung-bae Lee and Kopet. Appellants respectfully request that the rejection of claim 10 be reversed.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/IBM)

The rejection of claim 16 under 35 U. S. C. 103 (a), as being unpatentable over Jung-bae Lee, further in view of non-patent literature "Bit Vector Algorithm for detecting Self-Data Chains" (hereafter referred as "IBM"), is in error and should be reversed.

Claim 16

Claim 16 requires waiting a period of time appropriate to prevent conflicts between transfers of bytes for the first and second read operations and to minimize the amount of time between the ends of the burst transfer of data for the first read operation to the beginning of the burst transfer of data for the second read operation.

It is well established that obviousness requires a teaching or a suggestion by the relied upon prior art of all the elements of a claim (M.P.E.P. §2142). Without conceding the appropriateness of the combination, Appellants respectfully submit that the combination of Jung-bae Lee and IBM does not meet the requirements of an obviousness rejection in that it neither teaches nor suggests Appellant's invention as recited in claim 16.

However, the Final Official Action indicates without citing any legal precedent that a difference in sequence of a method does not change the purpose or functionality of the claimed invention. The Examiner appears to imply that the above indicated limitation of claim 16 has no effect on the functionality of the claimed invention. However, the limitation is more than just changing the order of various steps. The limitation to wait for an appropriate time was invented to prevent the conflict between transfer of bytes for the first and second read operations. Thus, the limitation of claim 16 includes a limitation not taught or suggested by the cited references.

Therefore, Appellants submit that the proposed combination does not arrive at the claimed invention nor render the claimed invention otherwise obvious. Appellants respectfully request the rejection of claim 16 be reversed.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/IBM/Carnevale)

The rejection of claim 17 under 35 U. S. C. 103 (a), as being unpatentable over Jung-bae Lee and IBM as applied to claim 16 above, further in view of Carnevale et al. (US Patent 5,721,874), is in error and should be reversed.

Claim 17

Claim 17 includes claim 16 as a base claim. Accordingly, claim 17 is allowable for at least the reasons stated above in regard to claim 16. In addition, claim 17 requires checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations.

In FIG. 8, Carnevale, discloses block diagram illustrating a page table arrangement for storing cache characteristic information for controlling cache access to configurable caches 12 and 22. Carnevale, also discloses the constructional and functional features of the page table. However, Carnevale does not appear to teach a process to check stored information relating to the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC. Jung-bae Lee and IBM also do not teach the limitation of claim 16.

As is well established, a prima facie showing of obviousness may only be established if there is a clear suggestion from or in the prior art to make the modifications proposed by the Examiner. *See Gillette Co. v. S.C. Johnson & Son, Inc.* 919 F. 2d 720 (Fed Cir. 1990). Appellants submit that there is no clear suggestion or motivation, in the light of the cited references, for a person to combine the references. The Official Action appears to combine the "Integrated Memory Circuit Device" of Jung-bae Lee and "Configurable Cache" of Carnevale in order to propose checking of the byte sizes, in order to improve system efficiency. Despite the broad statement made by the Examiner, there appears to be no motivation for one skilled in the art to make the proposed combination.

Since, the proposed combination does not teach checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations. Appellants respectfully request the rejection of claim 17 be reversed.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/IBM/Kopet)

The rejection of claims 18 and 19 under 35 U. S. C. 103 (a), as being unpatentable over Jung-bae Lee and IBM in view of Kopet et al. (US Patent 5,448,310), is in error and should be reversed.

Claims 18 and 19

Claims 18 and 19 include claim 16 as a base claim. Accordingly, claim 18 and 19 are allowable for at least the reasons stated above in regard to claim 16. Furthermore, Appellants submit that the above discussion regarding claim 16 is applicable to the patentability of claim 18 and 19.

Appellants respectfully submit that the combination of Jung-bae Lee, IBM and Kopet does not anticipate the invention of claims 18 and 19 and therefore the rejection of claims 18 and 19 be reversed.

Claim Rejections - 35 USC § 103 (Kopet/Ho-Cheol Lee/Keskar/Carnevale/IBM)

The rejection of claim 20 under 35 U. S. C. 103 (a), as being unpatentable over Kopet et al. in view of Ho-Cheol Lee, Keskar et al., Carnevale and IBM, is in error and should be reversed.

Claim 20

Claim 20 requires checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations.

As is well established, a prima facie showing of obviousness may only be established if there is a clear suggestion from or in the prior art to make the modifications proposed by the Examiner. *See Gillette Co. v. S.C. Johnson & Son, Inc.* 919 F. 2d 720 (Fed Cir. 1990). Appellants submit that there is no clear

suggestion or motivation, in the light of the cited references, for a person to combine the references.

The Official Action appears to combine the "Motion Estimation Coprocessor" of Kopet, the "Synchronous Dynamic Random Access Memory Device" of Ho-Cheol Lee, the "Programmable Memory Controller" of Keskar, the "Configurable Cache" of Carnevale and IBM's "Bit Vector Algorithm" to propose a memory IC having control logic shared by both the first and second groups of banks of memory, coupled to both the first and second row address decoders, coupled to both the first and second bank selection logics, storing information concerning the state of all banks in the first and second group separately. Despite the broad statement made by the Examiner, there appears to be no reason why one skilled in the art would arrive at the proposed combination.

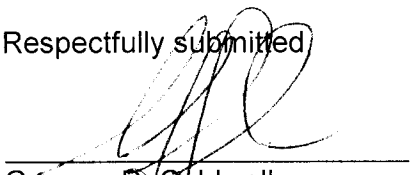
Carnevale teaches a page table arrangement for storing cache characteristic information for controlling cache access. However, Carnevale does not teach a process to check stored information relating to the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations.

Appellants submit that there is no suggestion or motivation, in the light of the cited references, for a person skilled in the art to combine the references. Therefore, a prima facie case of obviousness in regard to claim 20 has not been established. Appellants respectfully request the rejection of claim 20 be reversed.

CONCLUSION

In view of the foregoing, favorable reconsideration and reversal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner and/or the Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



January 26, 2007
Date

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(viii) Claims appendix.

What is claimed is:

1. (Currently Amended) A memory IC comprising:

a first group of banks of memory having a first bank, a first row address decoder coupled to the first bank, and a first bank selection logic coupled to the first row address decoder;

a second group of banks of memory having a second bank, a second row address decoder coupled to the second bank, and a second bank selection logic coupled to the second row address decoder, all able to operate independently of the first bank, first row address decoder and first bank selection logic;

a control logic shared by both the first and second groups, coupled to both the first and second row address decoders, coupled to both the first and second bank selection logics, storing information concerning the state of all banks in the first group, including the first bank, and separately storing information concerning the state of all banks in the second group, including the second bank; and

a data buffer shared by both the first and second groups.

2. (Original) The memory IC of claim 1, wherein the control logic and the data buffer cooperate to couple the memory IC to a memory bus and share access to the memory bus between the first and second groups, with the control logic receiving at least addresses and commands from the memory bus for memory operations involving both the first and second groups, and with the data buffer transferring data between the memory bus and both the first and second groups.

3. (Original) The memory IC of claim 2, wherein the control logic incorporates logic to arbitrate between the first and second groups for access to the data buffer to transfer data to and from the memory bus.

4. (Original) The memory IC of claim 1, wherein the control logic stores information concerning which rows are open in all banks in the first group separately from information concerning which rows are open in all banks in the second group.

5. (Original) The memory IC of claim 1, wherein a read transaction to read data from a row within the first bank is able to be timed and carried entirely independently of a read transaction to read data from a row within the second bank.

6. (Original) An electronic system comprising:

a memory IC having a first group of banks having a first bank, second group of banks having a second bank, control logic shared by both the first and second groups and having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group, and a data buffer;

a memory controller having a third state logic storing information concerning the state of all banks in the first group within the memory IC, and having a fourth state logic storing information concerning the state of all banks in the second group within the memory IC; and

a memory bus coupling the control logic and data buffer of the memory IC to the memory controller.

7. (Original) The electronic system of claim 6, wherein the control logic and the data buffer cooperate to share access to the memory bus between the first and second groups, with the control logic receiving at least addresses and commands from the memory bus for memory operations involving both the first and second groups, and with the data buffer transferring data between the memory bus and both the first and second groups.

8. (Original) The electronic system of claim 7, wherein the control logic incorporates logic to arbitrate between the first and second groups for access to the data buffer to transfer data to and from the memory bus.

9. (Original) The electronic system of claim 6, further comprising a processor coupled to the memory controller; and a cache utilized by the processor to store a subset of data stored in the memory IC.

10. (Original) The electronic system of claim 9, wherein the memory controller incorporates a control storage to maintain information concerning the size of a cache line within the cache.

11. (Original) The electronic system of claim 6, wherein the control logic stores information concerning which rows are open in all banks in the first group separately from information concerning which rows are open in all banks in the second group.

12. (Original) The electronic system of claim 6, wherein the control logic permits a read transaction to read data from a row within the first bank is able to be timed and carried entirely independently of a read transaction to read data from a row within the second bank.

13. (Original) The electronic system of claim 12, wherein the memory controller transmits addresses and commands to the memory IC for a first read transaction to read data from a first row within a bank in the first group and for second read transaction to read data from a second row within a bank in the second group, wherein the memory controller signals the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction, wherein the memory controller times the first and second read transactions to minimize the time that elapses between the end of the actual transfer of bytes across the memory bus for the first read transaction and the beginning of the actual transfer of bytes across the memory bus for the second read transaction.

14. (Original) The electronic system of claim 13, wherein the memory controller signals the memory IC that both the first and second read transactions are to be terminated early through indications of early termination embedded in the commands transmitted to the memory IC for both the first and second read transactions.

15. (Original) The electronic system of claim 13, wherein the memory controller signals the memory IC that both the first and second read transactions are to be terminated early through transmitting first and second burst termination commands across the memory bus, timed to indicate when to cease transferring further bytes of data for each of the first and second read transactions.

16. (Original) A method comprising:

selecting a first read operation to read data from a first row in a first group of banks in a memory IC;

selecting a second read operation to read data from a second row in a second group of banks in the memory IC;

determining a quantity of bytes to which each transfer of data will be limited for both the first and second read operations;

transmitting a first read command for the first read operation to the memory IC;

waiting a period of time appropriate to prevent conflicts between transfers of bytes for the first and second read operations and to minimize the amount of time between the end of the burst transfer of data for the first read operation to the beginning of the burst transfer of data for the second read operation;

transmitting a second read command for the second read operation to the memory IC;

receiving the burst transfer of data for the first read operation from the first row of the first group; and

receiving the burst transfer of data for the second read operation from the second row of the second group.

17. (Original) The method of claim 16, further comprising checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations.

18. (Original) The method of claim 16, further comprising signaling the memory IC that both the first and second read operations are to be terminated early through indications of early termination embedded in the commands transmitted to the memory IC for both the first and second read operations.

19. (Original) The method of claim 16, further comprising signaling the memory IC that both the first and second read operations are to be terminated early through transmitting first and second burst termination commands to the memory device, timed to indicate when to cease transferring further bytes of data for each of the first and second read operations.

20. (Original) A machine-accessible medium comprising code that when executed by a processor within an electronic system, causes the electronic system to:

interrogate a memory device to determine whether or not the memory device possesses banks of memory cells organized into a plurality of groups that permit independent memory operations;

configure a memory controller to make use of a memory device that possesses such independently operable groups of banks of memory cells;

check the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in a memory device that possesses such independently operable groups of banks of memory cells; and

determine a quantity of bytes to which to limit the burst transfer of bytes of data in a read transaction from a memory device that possesses such independently operable groups of banks of memory cells.

(ix) Evidence appendix.

None.

(x) Related proceedings appendix.

None.